What is claimed is:

1. A duty cycle correction circuit of a delay locked loop, comprising:

a differential amplifier having first and second input terminals and first and second differential output terminals, and adapted to receive differential reference clock signals input via the first and second input terminals, to amplify the differential reference clock signals, and to output the amplified differential reference clock signals via the first and second differential output terminals;

a first transmission circuit connected between the first differential output terminal of the differential amplifier and a first node, and adapted to transmit to the first node a first one of the amplified differential reference clock signals appearing at the first differential output terminal of the differential amplifier;

a second transmission circuit connected between the second differential output terminal of the differential amplifier and a second node, and adapted to transmit to the second node a second one of the amplified differential reference clock signals appearing at the second differential output terminal of the differential amplifier;

a first storage unit connected between the first node and a ground voltage, and adapted to store a signal of the first node;

a second storage unit connected between the second node and the ground voltage and adapted to store a signal of the second node; and

a switching circuit connected between the first node and a first output terminal of the duty cycle correction circuit, and connected between the second node and a second output terminal of the duty cycle correction circuit, the switching circuit having a control terminal adapted to receive a switching control signal to selectively

provide the signals of the first and second nodes to the first and second output terminals of the duty cycle correction circuit.

2. The duty cycle correction circuit of claim 1, wherein the switching circuit comprises:

a third transmission circuit adapted to transmit the signal of the first node to the first output terminal when the switching control signal has a deactivated state;

a fourth transmission circuit adapted to transmit the signal of the second node to the second output terminal when the switching control signal has the deactivated state;

a first voltage supplying circuit which is connected between the first output terminal and the ground voltage, and supplies the ground voltage to the first output terminal when a switching control signal has an activated state; and

a second voltage supplying circuit which is connected between the second output terminal and the ground voltage, and supplies the ground voltage to the second output terminal when the switching control signal has the activated state.

3. The duty cycle correction circuit of claim 2, wherein the first through fourth transmission circuits each include a PMOS transistor and a NMOS transistor.

4. The duty cycle correction circuit of claim 1, wherein the first and second storage units each include a MOS transistor.

5. A delay locked loop (DLL) comprising:

a DLL core adapted to receive an external clock signal and to generate an internal clock signal synchronized to the external clock signal;

a buffer adapted to buffer the internal clock signal and to output differential reference clock signals; and

a duty cycle correction circuit adapted to generate first control signals having desired offsets corresponding to differences in duty cycles of the differential reference clock signals, and to output the first control signals to the DLL core under the control of a switching control signal,

wherein the DLL core corrects a duty cycle of the internal clock signal in response to the first control signals.

6. The delay locked loop of claim 5, wherein the delay locked loop further comprises a pad adapted to receive the switching control signal.

7. The delay locked loop of claim 5, wherein the delay locked loop further comprises a mode register set for generating the switching control signal.

8. The delay locked loop of clam 5, wherein the buffer comprises a plurality of serially interconnected inverters adapted to generate the differential reference clock signals.

9. The delay locked loop of claim 8, wherein each of the plurality of inverters includes one PMOS transistor and one NMOS transistor, which are connected serially.

10. The delay locked loop of claim 5, wherein the duty cycle correction circuit comprises:

a differential amplifier having first and second input terminals and first and second differential output terminals, and adapted to receive the differential reference clock signals via the first and second input terminals, to amplify the differential reference clock signals, and to output the amplified differential reference clock signals via the first and second differential output terminals;

a first transmission circuit connected between the first differential output terminal of the differential amplifier and a first node, and adapted to transmit to the first node a first one of the amplified differential reference clock signals appearing at the first differential output terminal of the differential amplifier;

a second transmission circuit connected between the second differential output terminal of the differential amplifier and a second node, and adapted to transmit to the second node a second one of the amplified differential reference clock signals appearing at the second differential output terminal of the differential amplifier;

a first storage unit connected between the first node and a ground voltage, and adapted to store a signal of the first node;

a second storage unit connected between the second node and the ground voltage and adapted to store a signal of the second node; and

a switching circuit connected between the first node and a first input terminal of the DLL core, and connected between the second node and a second input terminal of the DLL core, the switching circuit having a control terminal adapted to receive the switching control signal to selectively provide the signals of the first and

second nodes to the first and second input terminals of the DLL core as the first control signals.

11. The delay locked loop of claim 10, wherein the switching circuit comprises:

a third transmission circuit adapted to transmit the signal of the first node to the DLL core when the switching control signal has a deactivated state;

a fourth transmission circuit adapted to transmit the signal of the second node to the DLL core when the switching control signal has the deactivated state;

a first pull-down circuit which is connected between the first node and the ground voltage, and pulls down the first node to the ground voltage when the switching control signal has an activated state; and

a second pull-down circuit which is connected between the second node and the ground voltage, and pulls down the second node to the ground voltage when the switching control signal has the activated state.

12. The duty cycle correction circuit of claim 10, wherein each of the first and second storage units includes a MOS transistor.

13. A duty cycle correction circuit, comprising:

a pair of input terminals adapted to receive a pair of differential reference clock signals each having a duty cycle;

integrating means for integrating each of the reference clock signals to produce a pair of control signals indicating the duty cycles of the differential reference clock signals; and

switching means adapted to receive a switching control signal and in response thereto to selectively output the control signals when the switching control signal has a first state and to output a pair of fixed voltage signals when the switching control signal has a second state.

14. The duty cycle correction circuit of claim 13, further comprising a differential amplifier adapted to amplify the differential reference clock signals and provide the differential reference clock signals to the integrating means.

15. The duty cycle correction circuit of claim 13, where the integrating means includes at least a pair of capacitors each for integrating a corresponding one of the reference clock signals.

16. The duty cycle correction circuit of claim 13, where the fixed voltage signals are ground voltages, and wherein the switching means includes a pair of transistors connected between corresponding output terminal and ground.